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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,625	05/03/2001	Paul M. Henry	50019.51US01/P04881	7855

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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,625	HENRY ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16* is/are allowed.

6)☒ Claim(s) *1-6,8,10-12 and 17-19* is/are rejected.

7)☒ Claim(s) *7,9,13 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *May 3, 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawing

The amendment and proposed drawing change submitted on Oct 18, 2002 were reviewed and considered with the following results:

The proposed drawing change was approved, and the objection to Fig. 9 has been withdrawn.

The applicants' comments indicate Figs. 3, 9, and 10 are correct, and page 4 states M1 "can operate in either direction" on page 4 of the amendment. Therefore, it is assumed the disclosed transistors within the application, and the claims, operate as resistive devices (unless they are disclosed as being diode-connected ones), allowing current to flow in either direction with respect to their source/drain. Since FETs are known to be bi-directional devices, their actual drain and source connections are not deemed critical. For example, it is known that if the gate of a P-channel FET is coupled to a low level (e.g. ground), it will conduct and act as a resistive device, and its source is typically considered the electrode coupled to the higher of the two voltage potentials connected to the transistor's source and drain electrodes. Also, unless specifically stated within a reference, the backgate (e.g. bulk, body, or substrate) of a P-channel FET is typically connected to either the transistor's source, or to the highest potential within the circuit. Assuming a specific example with a P-channel FET coupled between terminals A and B, wherein A has a higher potential than B, the transistor's electrode connected to terminal A could be deemed the source, and current would flow from A to

B. However, if B has a higher potential than A, the transistor's electrode connected to terminal B could be deemed the source, and current would actually flow from B to A.

However, the operation of the transistors is still not clearly understood with respect to what is shown. Therefore, the objections to the figures, with respect to their operation, are basically maintained with some exceptions (as previously described above). The drawing objections are described later with some modifications.

For reasons related to the above, the objection to how M1 would start conducting at startup has been withdrawn. Also, the objections to "M91 and "M92" on page 9 has been addressed by the amended change, and therefore has been withdrawn. However, how transistor M1 would turn off if its drain had a transient event, and how transistors M1 and M2 can be replaced by a single diode, have not been clarified. Therefore, the remaining operational related objections described in the previous Office Action have been maintained, and are described later with slight modifications.

The amended claims overcame all of the rejections of claims 1-7, and 14 as described in the previous Office Action. Those rejections have been withdrawn.

The amended claims, and comments, did not overcome the prior art rejections of claims 1-6, 8, 10-12, 17, and 18 with respect to Tailliet. Those rejections have been modified, with respect to the amended changes, and are described later under the appropriate section. Related comments are described under the Response to Arguments section. Also, newly added claim 19 is included in the prior art rejections.

Drawings

The drawings remain objected to because it is believed the connections of the P-channel transistor(s) (e.g. see M1 of Fig. 3; M1 and M2 of Fig. 4; M91 of Fig. 9; and M101 and M102 of Fig. 10) are either incorrectly shown, or their operation is not described correctly. As presently shown, it is not believed the transistors will turn-off as described within the specification. For additional details, see the related objections under the Specification section. Therefore, a proposed drawing correction or corrected drawings, and/or clarification, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: It is still not clear how M1 (shown in Fig. 3) would turn off if its drain's supply signal had a transient event (i.e. sharp, temporary drop in voltage). Since capacitor C1 would be fully charged to the normal level of the supply signal during normal operations, it would appear the source (e.g. at node 320) of M1 would still have a higher voltage than ground, which is coupled to the gate of M1. If this is the case, M1 would continue to conduct, but this time allowing current to flow from the higher potential (the charge on node 320) to the lower potential (temporarily on 310). Therefore, clarification is requested with respect to how the circuit can actually be turned off with the connections shown in Fig. 3. Similarly, clarification is requested with respect to how transistors M1 and M2 would actually function (e.g. see Fig. 4 and page 6, line 19 through page 7, line 9). For

example, the examiner requests a clear description of, and/or a prior art reference that clearly shows and describes, the operation of two P-channel transistors coupled together (in series) by their sources. Page 7, lines 10-11 have not been satisfactorily clarified. It is still confusing because it indicates both transistors M1 and M2 are replaced by a single diode without clearly citing how the transistors operate. For example, a diode can be considered one type of resistive device, but a resistive device is not necessarily a diode. Therefore, clarify how these two transistors can be replaced by a single diode. Also, for the same reasoning as applied to the P-channel transistor of Fig. 3, clarification is requested with respect to the operation of transistor M91 as shown in Fig. 9 with its drain connected to receive the logic signal, and its source connected to capacitor C91. For example, it is believed capacitor C91 will charge to a high logic level with respect to a high Logic Signal during normal operations. However, if the high Logic Signal has a low transient (short, sudden drop with respect to the high level), the charge on C91 will be provided to line 910, and will also be provided to line 905 through resistive means M91,M92 (M91 is a P-channel transistor with its gate coupled to a low; M92 is an N-channel transistor with its gate coupled to a high). The same type of objections to the operations of the circuits, with respect to the transistors shown in Figs. 3, 4 and 9, also apply to the circuits shown in Figs. 5-7 and 10. Appropriate corrections and/or clarifications are required.

Claim Objections

Claims 8-13 are objected to because of the following informality: It is suggested "second signal" on line 7 of claim 8 have --the-- added prior to it since "second signal"

was already cited on line 6. Also, it is noted that claim 8, line 7 clearly associates both the "first" and "bias" signals with their own "the." [This objection was inadvertently overlooked (left out of the previous Office Action).] Claims 9-13 carry over the objection from claim 8. An appropriate correction is required.

Claim Rejections under 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 10-12, 17, and 18 remain rejected, and newly added claim 19 is rejected, under 35 U.S.C. 103(a) as being unpatentable over Tailliet. In Fig. 2, Tailliet shows an apparatus comprising a signal transfer circuit 1 arranged to receive a supply signal Vdd and output a first signal Sd to a pin A of circuit 3 and also to charge storage circuit C2. Although the reference does not clearly describe normal and transient event

operations, one of ordinary skill in the art would understand (e.g. find it obvious) that charge storage circuit C2 would be fully charged to Vdd by first signal Sd when the circuit is operating normally (e.g. transistor T1 of transfer circuit 1 acts as a resistive device when Vdd is applied; and when Vdd is stabilized (e.g. during normal operation)). When a (negative) transient event occurs on supply signal Vdd (e.g. Vdd temporarily drops below either the switching threshold level of transistor T1, or the normal level of the voltage on pin A), charge storage circuit C2 will provide its stored charge (e.g. equivalent to the fully charged, stable level of Vdd) as the second signal to provide power (e.g. voltage) to pin A of circuit 3 during the transient event. Therefore, it would be obvious to one of ordinary skill in the art that circuit 3 would be considered protected from a sudden, short transient event, thus rendering claims 1 and 2 obvious. In this case, the circuit is protected from inadvertently changing the logic state of signal POR during a temporary (negative) transient of supply signal Vdd. Since Tailliet shows signal transfer circuit 1 with transistor T1, and also discloses the use of diode-connected transistors with respect to transistor T1 (i.e. transfer circuit 1) on column 4, lines 63-65, claims 3 and 4 are rendered obvious. Also, the charge storage circuit C2 is shown comprising capacitor circuit C2, rendering claims 5 and 6 obvious. [Note that one of ordinary skill in the art would know capacitor circuit C2 would be sufficient in size to hold enough charge during a transient event (understood to be a very short, temporary fluctuation), otherwise circuit 3 could inadvertently switch its logic state during the transient event. Such an inadvertent switching could change the level of POR output signal when it isn't necessary.] Since signal transfer circuit 1 functions as a resistive

device during normal operations, it maintains (i.e. prevents) the stored charge on charge storage circuit C2 from falling below the power level on pin A, thus rendering claim 19 obvious. Interpreting Fig. 2 slightly different, the figure shows signal transfer circuit 1 receiving supply signal Vdd and outputting first signal Sd; charge storage circuit C2 receiving a bias signal from bias circuit 2 (e.g. see column 3, line 49) and first signal Sd; inverting circuit 4 receiving the first signal (from 1), the second signal (from C2) and the bias signal (from 2), wherein inverting circuit 4 is coupled to a pin (e.g. input) of circuit 5,6. During normal operations and a transient event, the pin will be held low (because node A will be high), and during startup it will be high (since node A will initially be low), thus rendering claims 8, and 10-12 obvious for the same reasons as previously described with respect to claims 1-6. Signal transfer circuit 1 is a means for receiving supply signal Vdd; 1,C2 comprise means for determining when normal operations and transient events occur (e.g. under normal operations, signal transfer circuit/means 1 provides a first signal to pin A of circuit 3 to keep C2 charged to Vdd, and during a (negative) transient event of supply signal Vdd, charge storage circuit/means C2 provides a second signal (a charge equivalent to the level of Vdd during normal operations), as a power (e.g. voltage) to pin A of circuit 3 to allow the circuit to maintain its logic output state during the transient event. Therefore, Fig. 2 renders method claim 17 and apparatus claim 18 obvious.

Allowable Subject Matter

Claims14-16 are allowable. There is presently no motivation to modify or combine any prior art reference(s) to ensure the apparatus comprises the

complementary switch and charge storage circuit combination/relationship as recited within independent claim 14 (upon which claims 15 and 16 depend), wherein it is presently interpreted that the switch receives the input logic signal at its input, and provides the output logic signal at its output.

Claims 7, 9, 13, and 20 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the transistor circuit comprises the first and second transistors as recited within claims 7 and 13; 2) the inverting circuit is a Schmidt trigger as recited within claim 9; and the body connection of the transistor circuit is coupled to the pin of the circuit as recited within newly added claim 20.

Response to Arguments

The applicants' comments/arguments filed Oct 18, 2002 have been fully considered but they are not persuasive. The applicants comment and/or argue that: 1) the operation of the transistors have been clarified; 2) transistors M1 and M2 can be replaced by a single diode; and 3) the amended claims cite the second signal provides "power", and Tailliet doesn't include this limitation.

1) Without clearly explaining (or pointing out in the disclosure) the details of operation with respect to the examiner's request for clarification, the applicants state they believe the transistor's operation has been clarified. However, if a capacitor on one electrode of a normally conducting transistor is allowed to fully charge to a high

potential applied to another electrode of the transistor, then wouldn't the transistor continue to conduct current (but in the opposite direction with respect to the electrodes original direction) if the potential on the another electrode temporarily drops due to a transient event? Therefore, clarification is still requested that will clearly address the concerns described by the examiner with respect to how the transistor(s) can operate (e.g. turn off) as presently shown/disclosed.

2) The examiner had also requested clarification with respect to replacing M1 and M2 with a single diode. However, the applicants' merely state "This is a correct interpretation. Transistors M1 and M2 may be replaced by a single diode" on page 5 of the amendment. This clarification is considered insufficient. As presently understood, and basically admitted by the applicants' phrase "can operate in either direction", it is believed transistors M1 and M2 would allow current to flow from 310 to 320 when the voltage on 310 is higher than the voltage on 320, and until C1 become fully charged. However, once C1 is fully charged, current flow would cease to capacitor C1. When a (negative) transient on 310 occurs, transistors M1 and M2 would conduct current from 320 (the higher potential) to 310 (the lower potential). Therefore, without clear operational details of M1 and M2, it is not understood why these two resistive devices would be replaced with one diode.

3) The applicants' argument with respect to "power" fails to comply with 37 CFR 1.111(b) because it amounts to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Although the applicants indicate

Taillet's capacitor C2 aids in detecting a POR, and does not provide power to a circuit's pin, the examiner disagrees with the "power" interpretation. One of ordinary skill in the art knows that a voltage charge held by a capacitor is one type of power. For example, Taillet's power signal Vdd has a voltage level equivalent to Vdd. This power signal can be considered a power supplied to Taillet's overall circuit. Since capacitor C2 becomes fully charged to voltage Vdd during normal operations, it will provide voltage/power Vdd to pin A of circuit 3 during a (negative) transient on power signal Vdd as described within the rejections.

Therefore, the objections, rejections under 35 U.S.C. 112, and the prior art rejections are deemed proper as described above.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

11 January 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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